



ACE Global Engineering Network
Electronics Industry

ACE Global Engineering Network

Electronics Industry

Contents

Occupancy Overview	1
Process Flow	1 - 2
Classification	2
Special Hazards	2
Other Semiconductor Special Hazards	2
Manufacturing printed circuit boards	2
Manufacturing printed wiring assemblies	3
Manufacturing of TFT-LCD panels	3
Earthquake	4
Business Interruption and Contingent BI Considerations	4 - 5
Industry Trends	4
Requirements	5
Industry Benchmarking	6
Industry Loss Information	7
ACE Contacts	7
Reference Sources	7





Occupancy Overview

The Electronics industry includes the manufacture of: passive components (resistors, capacitors, inductors) semiconductors components (discretes, integrated circuits) printed circuit boards (single and multi layer boards) printed wiring assemblies TFT-LCD (thin-film transistor – liquid crystal display) panels

The manufacturing of passive components is similar to the manufacturing of semiconductors, although passive component manufacturing uses fewer toxic chemicals in doping semiconductor components and more organic solvents (epoxies, plating metals, coating and lead).

'Electronics' covers a wide range of risks, due to unique features such as the extremely high values involved and special hazards. Since many other electronic businesses are closely related to semiconductor manufacturing, this ACE Industry Fact Sheet focuses on the semiconductor industry.

Computer chip technology influences the manufacture of an increasing range of everyday items, from space crafts to coffee makers, traffic lights to computers. The simple test is: if a device uses electricity and you can 'tell it what to do', there's a chip inside. A microprocessor is the most complex manufactured product on earth – taking hundreds of steps to make in the world's cleanest environments.

Process Flow

Process flow for semiconductor manufacturing is best considered in two sections: *front-end* and *back-end*.

The *front-end* is wafer processing, performed in a *Wafer Fab* area.

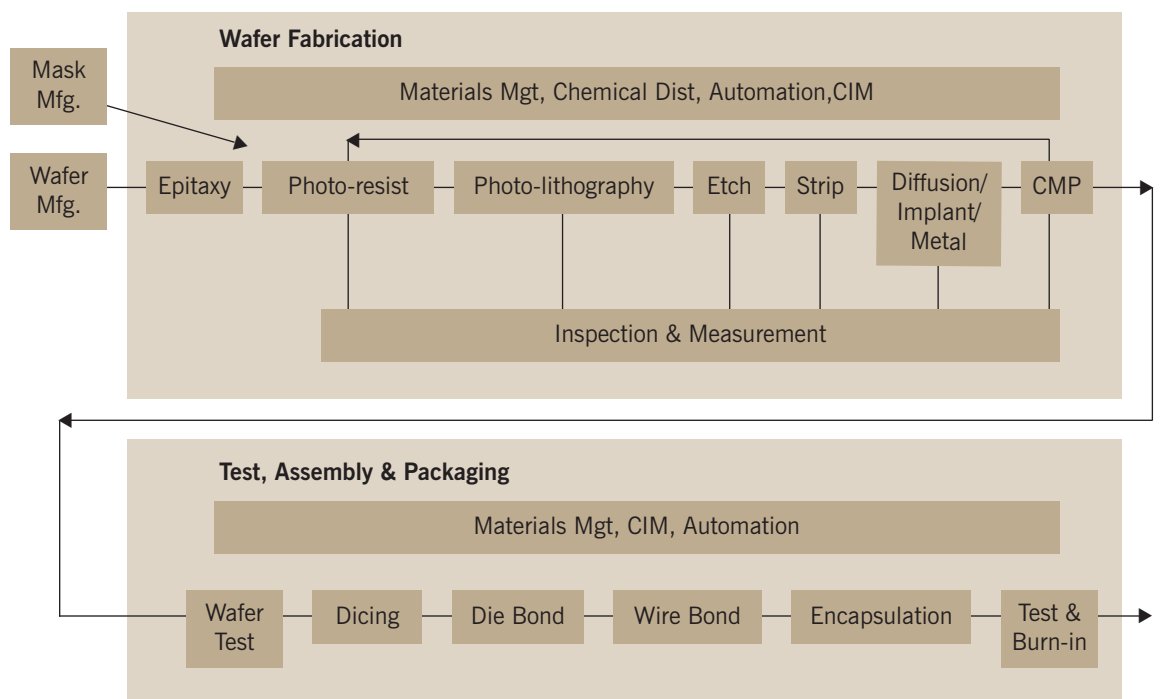
Semiconductors are produced by treating semiconductor substances with dopants such as boron or phosphorous atoms to give them electrical properties. Important substances are silicon and gallium arsenide.

The process of wafer fabrication is a series of loops, each stage depositing a layer on the device. The stages include:

- Crystal growth
- Acid etch and epitaxy formation
- Doping and oxidation
- Diffusion and ion implantation
- Metallisation
- Chemical vapor deposition
- Die separation
- Die attachment
- Post-solder cleaning
- Wire bonding, encapsulation packaging
- Final testing, marking and packaging.

Several process steps are repeated and the sequences may well exceed a hundred process steps. So each loop comprises some or all of the major steps of the following process:

- Silicon wafer and mask manufacturing (not typically done at a semiconductor plant)
- Photolithography
- Etch
- Strip
- Diffusion
- Ion implantation and/or deposition
- Chemical mechanical planarisation.



www.Electros.in

At each stage, various inspections and measurements monitor the process and equipment. The entire process in turn is supported by a complex infrastructure of materials supply, waste treatment, support, logistics and automation.

The cleanroom Fab requires the cleanest environment in the world many times cleaner than the best hospital operating theatre. Consequently a Fab is one of the most complex industrial facilities ever developed. A state-of-the-art Fab, costing over \$1 billion, has a denser capital per square foot than any other industry.

The *back-end* process is 'test, assembly and packaging': the finished wafer is split up into

individual die (chips) which are then assembled into packages which can be handled in the final applications. Full functional electrical testing is performed at both wafer and package level to ensure outgoing quality.

Classification

ICC	NAIC	SIC	Class
3671	334413	3674	5, 7

Note:

- Europe/Asia is using Class 5 for Front End and Class 10 for Back End manufacturing.
- NAICS uses Class 7 which should be adjusted accordingly to reflect the hazards of the industry.

Special Hazards

The process hazards of manufacturing semiconductor devices arise from the extensive use of:

- Toxic gases
- Highly corrosive gases and liquids
- Flammable gases
- Flammable liquids
- Pyrophoric gases such as Silane.

The extensive use of combustible plastics adds to the high risk of fire loss. Because the process equipment is expensive and the product in process is extremely susceptible to fire, smoke and water damage, there is great potential for substantial loss from fire, even if it is confined to a very small area.

The production also involves carcinogenic and mutagenic substances and consequently production is largely carried out in closed systems.

Heating equipment in conjunction with plastic materials, such as wet benches, are used extensively in Fabs (new FM approved plastics are now on the market – see Industry Trends).

Silane – more than any other gases used in semiconductor manufacturing – can lead to severe explosions. Although a stable gas it is pyrophoric and so, under certain conditions, can spontaneously ignite or result in delayed ignition leading to an explosion. Silane has caused a considerable number of fires and common scenarios include: untreated Silane released into combustible fume-exhaust ductwork and improper cylinder change-out procedures resulting in leaks at the cylinder connection.

Other Semiconductor Special Hazards

- Plastic-heated corrosive wet benches – gaseous or fine mist is required activated by flame detection or FM-approved plastic materials
- Stainless steel solvent wet benches – gaseous or fine mist is required activated by flame detection
- Bulk Hydrogen delivery systems
- VOC (Volatile Organic Compounds) thermal burn systems used to burn off waste gases – typically gas fired
- Exhaust systems for corrosive gases using plastic ducts – sprinklers required or FM 4910 plastics
- Flammable liquid waste collection systems
- Smoke contamination issues – air-sampling, smoke-detection systems required. These are arranged to operate a dedicated smoke removal system or shut-off cleanroom air re-circulation fans by zone automatically or manually with adequate fire team response. They also divert smoke to the outside atmosphere and operate make-up air vents (minimum 3 cfm per sq. ft. [0.9 m³/min per m²] ventilation rate 0.

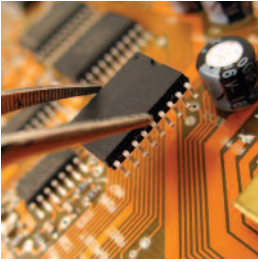
- Front-opening unified pod (FOUP) – these are plastic containers which protect the costly silicon wafers during production. Each FOUP can hold up to 25 wafers, representing more than US\$100,000 worth of product. New FM Approval Standard 4911: Wafer carriers for use in cleanrooms.

Manufacturing printed circuit boards

There are three types of board:

- single-sided boards (circuits on one side only)
- double-sided boards (circuits on both sides)
- multilayer-boards (three or more circuit layers)

Board manufacturing is achieved by producing patterns of conductive material on a non conductive substrate by subtractive or additive processes. The conductor is usually copper; the base can be pressed epoxy, Teflon, or glass. The subtractive process is the preferred method and includes; cleaning and surface preparation of the base, electroless copper plating, pattern printing and masking, electroplating and etching.



Manufacturing printed wiring assemblies

Printed wiring assemblies consist of components attached to one or both sides of the printed circuit board (PCB). Attachment is by 'through-hole technology' in which the legs of the components are inserted through holes in the board and soldered in place underneath, usually with a tin alloy.

The alternative is Surface Mount Technology (SMT) where components are attached to the surface by solder or conductive adhesive.

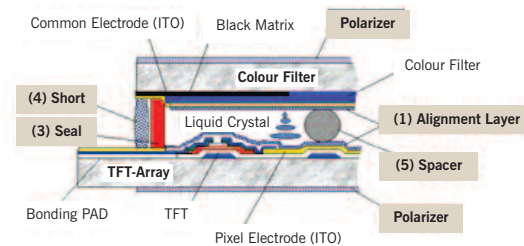
PCBs of all types may require drilled holes to be copper plated to ensure interconnections between the different copper layers.

Manufacturing of TFT-LCD panels

TFT-LCD panel manufacture consists of several processes, including: array, colour filter and cell, and module assembly operations. The array operations are almost identical to those for manufacturing semiconductors, except there is no ion-implantation process. Glass panels are used as a substrate instead of silicon wafers. There are fewer varieties of hazardous chemicals/gases used in the process but the quantities used are much greater than in semiconductor manufacturing.

The TFT-LCD panel is just like a sandwich panel (don't understand). The thin-film transistor is generated on the back panel through the array process. The colour filter is produced on the front panel by processes such as BM (black matrix) coating, RGB (red, green, blue) coating and ITO (indium tin oxide) sputtering operations. The space between the two panels is controlled by spacers and is then filled with liquid crystal, guided by the patterns formed by PI (polyimide) coating, rubbing and drying operations. The module assembly equips the sandwich panel with polariser, driver ICs, flexible PCBs, backlighting, and frames.

The structure of a TFT-LCD Panel



www.avdeals.com/classroom/fabricating_tft_lcd.htm

The colour filter and cell processes are all carried out in clean rooms. Various flammable liquids are used, such as PGMEA (propylene glycol mono-methyl ether acetate) and NMP (n-methylpyrrolidone). Apart from the array process, no hazardous gases are used in other TFT-LCD manufacturing processes. In Wafer Fabs, the plain wafer, WIP and finished products are generally placed in PC cassettes/boxes. In TFT-LDC plant, the glass substrates and glass panels without module assembly are stored in combustible PP (polypropylene) boxes. Some of the empty PP boxes are stored in the clean room owing to the concern of contamination, but increasing the fire load in the clean room.

The high production demand means that process gases, including silane and ammonia, are generally supplied by Y-cylinders (also known as 450-L tonners). In most cases, the silane Y-cylinders are placed in an open area fenced by open chain link fences. The area is well detached from the Fab building and provided with either automatic deluge water spray or wet-pipe sprinkler systems.

In addition, a high-rise automated storage and retrieval system (ASRS) warehouse is generally installed in the plant to store semi-finished and finished products, due to the bulk of the panels. Other critical issues include the effectiveness of ceiling sprinkler and in-rack sprinkler systems designed for the warehouse and fire cut-off between the warehouse and its adjacent areas.

Earthquake

Surprisingly and coincidentally, the highest concentration of semiconductor fabs are situated in three of the most earthquake-prone regions in the world: Japan, Taiwan and California. Highly specialised and sensitive semiconductor processes and equipment are extremely susceptible to earthquake damage.

Significant damage occurred during the September 1999 Taiwan earthquake resulting from vertical diffusion quartz tube breakage and lengthy power cuts of up to a week in the Hsin-chu Science Park.

If earthquake coverage is provided, the following requirements and provisions should be considered for older Fabs:

- A seismic risk management programme managed by a specialist, independent consulting firm.
- An earthquake contingency plan for rapid regeneration after the incident
- All tools and equipment seismically braced and raised pedestal floors strengthened to withstand a 1:500-year-return-period earthquake (criteria - UBC97)
- Seismic detectors, arranged to shut off hazardous gases – typically so that two out of three detectors shut down hazardous gas systems
- Back-up supply of quartz tubes used in CVD and diffusion furnaces. Trained emergency repair contractors should also be appointed
- Structural seismic design targeting seismic resistance to acceptable levels (i.e. 49 g)
- Sprinkler system earthquake sway – bracing required in accordance with NFPA 13
- All critical tools and facility systems equipped with UPS and emergency generators
- Back-up power supply to be adequately maintained and serviced, including annual thermograph scanning programme (100% power back up should be the goal).



Business Interruption (BI) and Contingent BI Considerations

Chips are susceptible to even the tiniest speck of dust. As a result cleanrooms have proved difficult areas to protect from fires: by the time a cleanroom fire triggers a sprinkler or special fire-protection system, damage will have already occurred. Contamination from a fire, no matter how small, can put a chipmaker out of business for weeks, if not permanently.

The semiconductor industry is a global undertaking, with even US facilities often depending on key suppliers based in Asia and Europe. An interruption at a plant in Taiwan can therefore have a business interruption impact at a facility in California.

All major semiconductor Fabs should have a complete business continuity plan in place.

Industry Trends

- 12" (300 mm) wafers offer 125% greater surface area than standard 8" (200 mm) wafers and an estimated 40% reduction in manufacturing costs. It is now estimated that semiconductor manufacturing equipment comprises nearly 75 percent of the cost of new semiconductor fabrication plants.
- Growth in the semiconductor materials market has been positive for the past six years. Wafer fabrication materials are expected to drive a large percentage of future growth due to investments in 300 mm Fabs over the past year. The outlook changed drastically in September 2008, proving how strongly the industry is tied to the health of the world economy but prospects for growth in 2009 seems more positive.
- The capacity-output factor per plant will be increased due to high investment costs and return on investments. This puts greater pressure on BI cover and, for multinational companies, contingent BI becomes more critical.
- Different generation technologies used in the production of TFT-LCD panels apply different dimensions of mother (plain) glass substrates. For example, 6th generation technology uses glass substrates measuring 1,500 mm x 1,850 mm. The most advanced technology – 10th generation – will use glass panels of 2,850 mm x 3,050 mm. This means that the size of clean room will increase accordingly from a 6th generation Fab building, currently around 300 m x 150 m.
- Fire protection in the semiconductor Industry has improved significantly over the past ten years due the following:
 - Increased capital spending on safety
 - Fire-safety construction materials
 - Better fire detection and suppression
 - Combustible duct replacement/sprinklers
 - Improvements in codes and standards (NFPA 318, FM 7-7, SEMI)
 - Improved process heating systems

However, there are still several major concerns as follows:

 - Still many Fabs with combustible ducts without protection
 - Not all Fabs are fully sprinkler protected (especially in Asia)

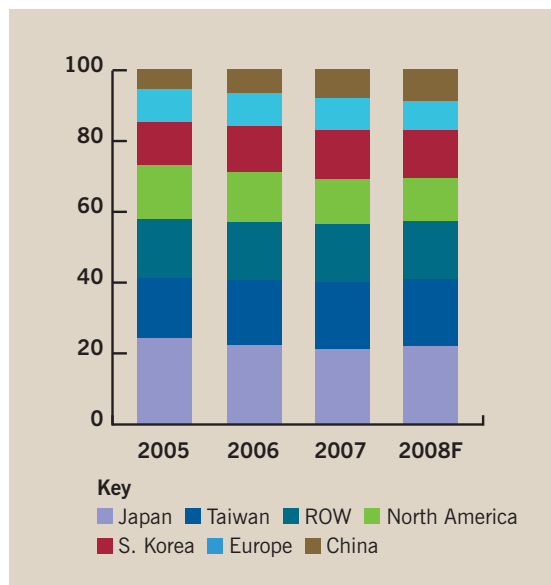


- Difficulties in retro-fitting existing Fabs with sprinklers due to loss of production
- Inadequate fire cut offs between departments within clean rooms to allow for smoke control.
- FM Approvals' specification test standard, known as FM4910, is a test procedure that evaluates the fire hazards of engineered plastic materials designed for use in the manufacture of cleanroom products. Materials that meet the 'Clean Room Materials Flammability Test Protocol' do not specifically require fixed fire protection when used according to the appropriate FM Global data sheets. FM4910-listed materials may burn locally in the ignition area but will not propagate a fire beyond that zone. Additionally, such materials produce little, if any, smoke or corrosive byproducts, thus minimizing non-thermal damage

An FM 4910 tool is now a standard order. A non 4910 tool is now a special order. Today, there are 17 manufacturers producing nearly 150 different types of FM4910-listed materials. A complete listing of FM4910 materials can be found at www.fmglobal.com/assets/pdf/4910Approved.doc

- In May of 2008, Intel, Samsung Electronics and TSMC announced 'an agreement on the need for industry-wide collaboration' to target a transition to larger, 450mm-sized wafers starting in 2012
- International HPR insurance carriers are reportedly moving into this market, now that the semiconductor industry in Taiwan follows internationally recognised NFPA 318 and FM 7-7 for new Fabs and have upgraded many older Fabs to meet these standards.

Regional Market Share for Semiconductor Materials Market (2005 – 2008)



Source: Materials Market Data Subscription, November 2008.
ROW – Rest of World

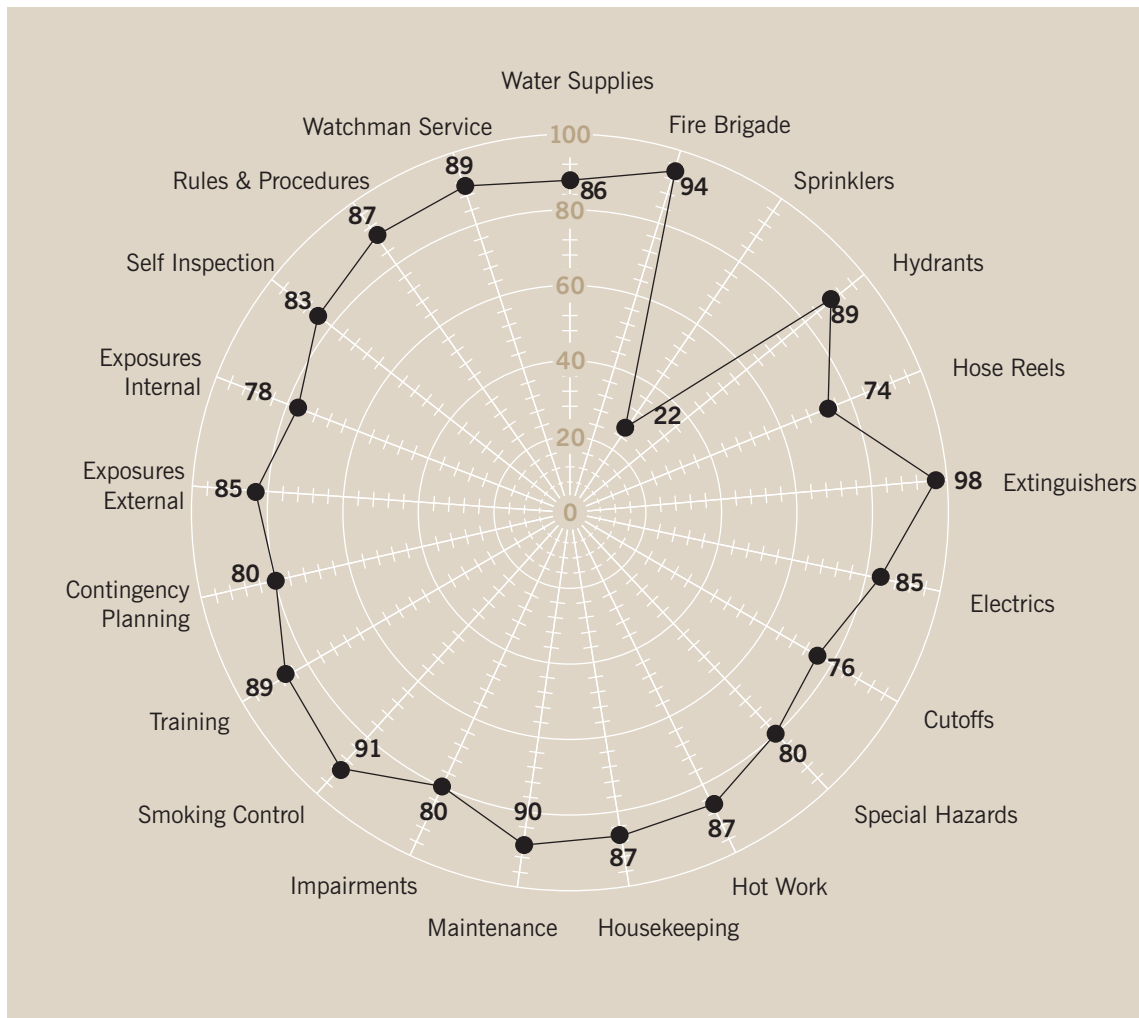
Requirements

- Complete sprinkler protection
- Compliance with FM 7-7 and NFPA 318
- Must have strong risk-management programme in place
- Annual servicing frequency, due to high values and special hazards.

Industry Benchmarking

Outer circle represents best industry practice.

Black line represents the global average of ACE inspected electronics facilities during a period of five years.



Industry Loss Information

Date	Company	Loss Estimate	Loss
1996	Winbond Taiwan	\$200 M (US)	Fire – Silane Gas leak CVD machine
1997	UICC Taiwan	\$380 M (US)	Fire during work on polypropylene duct, spreading to other areas via exhaust and ventilation system
1997	Lien-Juan	\$400 M (US)	Fire – Silane leak Integrated Circuit
1999	Taiwan Earthquake	\$8 M – PD but over \$500 M in BI	Physical Equipment Damage & BI
2000	UMC Taiwan	\$1 M (US)	Fire – Generator overheated
2003	Philips Caen France	~ 190 mio Euro	Fire in Plastic Duct
2005	Advanced Semiconductor – Taiwan	\$270 M (US)	Fire

A Taiwan based study outlines losses as follows: fire (40.7%), leakage (33.3%), explosion (11.1%), electricity interruption (7.4%), water interruption and leakage (3.7%) and earthquake (3.7%). Based on its data the study also makes the following estimates

- One in ten Fabs suffers a fire loss annually
- The overall industry standard is one in 100
- Average fire loss in semiconductor industry is \$8,000,000 (US)
- Average fire loss in general industry is \$250,000 (US)

Source – FM Study

ACE Contacts in your region for further information:

Name	Region	Office	Contact Information
Meg Liu	Asia Pacific	Taipei, Taiwan	Meg.Liu@acegroup.com Phone: + 886 (2) 8758 1832
Rick Gerbrandt *G	Canada	Vancouver, Canada	Rick.Gerbrandt@acegroup.com Phone: + 1 604 895 7467
Steven Elshout	Europe	Rotterdam, Netherlands	Steven.Elshout@acegroup.com Phone: + 31 (010) 289 3518
Joel Marin	Latin America	Mexico City, Mexico	Joel.Marin@acegroup.com Phone: +52 55 52585800
Bruce Redepenning	USA	Minneapolis, USA	Bruce.Redepenning@acegroup.com Phone: +1 (612) 721-8684

*G – Denotes Global Product Champion

Reference Sources

FM 7-7

NFPA 318

www.semi.org

www.electros.in

Materials Market Data Subscription, November 2008



ACE Global Engineering Network

The ACE Global Engineering Network creates strong, long term relationships with clients, focusing on cost effective and proficient solutions to their risk management challenges.

Through in depth loss prevention training backgrounds and industry expertise, ACE engineers are experienced in evaluating a wide variety of risks and complexity of exposures.

Our specialist team is driven by account and field engineers delivering high quality and effective loss prevention services. We have engineers in key strategic locations around the world who are familiar with international standards as well as local codes and work practices. This proves invaluable in helping clients establish and maintain operations in traditional and emerging markets.

For further information please go to: www.aceagen.com